Improved low reflection transition from microstrip line to empty substrate integrated waveguide

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***Abstract*—Substrate integrated waveguides (SIW) maintain the advantages of planar circuits (low loss, low profile, easy manufacturing, integration in a planar circuit board), and improve quality factor of filter resonators. Empty substrate integrated waveguides substantially reduce the insertion losses because waves propagate through air instead of through a lossy dielectric. The first empty substrate integrated waveguide (ESIW) used a simple tapering transition that can not be used for thin substrates. A new transition has recently been proposed which includes a taper also in the microstrip line, not only inside the ESIW, and so it can be used for all substrates, although measured return losses are only 13 dB. In this work the cited transition is improved by placing via holes that prevent undesired radiation, as well as two holes that help to ensure good accuracy in the mechanization of the input iris, thus allowing very good return losses (over 20 dB) in the measured results. A design procedure, that allows the successful design of the proposed new transition, is also provided. A back to back configuration of the improved new transition has been successfully manufactured and measured.**

***Index Terms*—Substrate integrated waveguide, empty substrate integrated waveguide, planar circuits, transition, tapering structures.**

I. Introduction

Substrate integrated waveguides have attracted much attention in the last years because they maintain the advantages of classical planar circuits, but they outperform planar circuits in terms of higher quality factor for resonators and filters. The quality factor, as well as the insertion losses, can be improved if the dielectric is removed. Thus, several substrate integrated lines without dielectric have appeared, such as the empty substrate integrated waveguide (ESIW) [1], the hollow substrate integrated waveguide (HSIW) [2], the air filled substrate integrated waveguide [3], the dielectricless substrate integrated waveguide presented in [4], or the empty substrate integrated coaxial line (ESICL) [5]. The cited ESIW has already been successfully tested with the design and manufacturing of coupled cavity filters with very high quality factors, a horn antenna, and a hybrid directional coupler. All these devices are connected to microstrip accessing lines through the microstrip to ESIW transition originally presented in [1]. This transition has proved to perform satisfactorily, but its performance can still be improved. Besides, for thin substrates, the optimum values of w_{ti} and l_t (see figure 1(a)) produce a very long and narrow taper than cannot be manufactured, so this taper cannot be used in those cases.

In [6] a new transition from microstrip to ESIW is presented. It is the same transition as the one presented in [1] (see figure 1(a)), but it includes an additional taper in the microstrip line (see figure 1(b)). With this additional taper good results are achieved also for thin substrates. But measured return losses are only of 13 dB, and no design procedure is provided.

In this work, the new transition of [6] is improved by mechanizing via holes that avoid power leakage, as well as two holes that ensure good accuracy in the dimensions (w_{ir}) of the manufactured input iris (see figure 1(c)). The accuracy of this iris is crucial for ensuring good impedance matching and low return losses, and good agreement between simulated and measured return loss results. A back to back transition is manufactured, and measured return loss is over 20 dB in the whole frequency band of the fundamental mode. Besides, in this work a design procedure is presented, which provides with a very good starting point for all the design parameters of the new transition, thus easing a good and easy convergence to the optimal design.

II. Design procedure

The first time that the ESIW was presented in [1], the connection of the ESIW to the accessing microstrip lines was solved with the transition of figure 1(a). This transition consists on a tapering structure inside the ESIW that decreases the dielectric of the microstrip line exponentially until it disappears. Good initial values for the design parameters (l_t, w_{ti}, w_{ir} and c) are provided in [1] (c controls the exponential curve of the taper). An optimization is next used to fine tune the design parameters, and simulated return losses of around 20 dB are obtained with this transition.

In [6] the transition is improved with an additional taper in the microstrip line, as shown in figure 1(b). Parameters $l_{t_{ms}}$ and $w_{t_{ms}}$ control the dimensions of this additional taper. This transition is still improved in this work with the mechanization of two holes of diameter d_f (see figure 1(c)). These holes, mechanied with the drilling machine, ensure that the size of the opening in the back wall of the ESIW is exactly of width w_{ir}. Otherwise, the width w_{ir} that is obtained with the drill in the structure of figure 1(b) has large tolerances and deviates the measurements from the simulation, as happens in [6]. Finally, via holes of diameter d_v and pitch s_v (see figure 1(c)) are mechanized in order to prevent possible leaky waves traveling through the substrate outside the ESIW. d_v and s_v are chosen to avoid radiation leakage with the same design rules as for the vias in a standard SIW [7].

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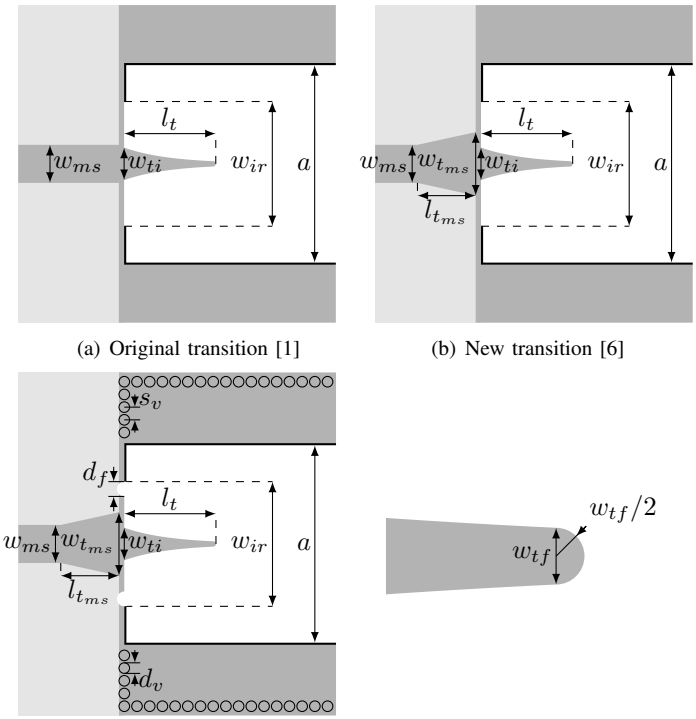


(a) Original transition [1] (b) New transition [6]

(c) Improved new transition (d) Detail of the taper end

Fig. 1. Original [1], new transition [6] and the improved version of the new transition presented in this work. Dark gray is dielectric substrate; light gray represents the copper metallization on top layer; black represents the border metallization which has been used to close the ESIW; and white is air.

In order to design the proposed transition, it is convenient to find a good initial point for the design parameters. Table I lists expressions that provide good approximations for the design parameters, and that can be used to obtain a good initial point. These expressions have been obtained experimentally after designing the transition for different frequency bands and different substrates, with long optimization processes using robust genetic algorithms. The initial point proposed can speed up significantly the optimization process for new designs, regardless of the frequency band, or the specific substrate that is chosen for each case.

l_t	w_{ti}	w_{ir}	c	$l_{t_{ms}}$	$w_{t_{ms}}$
$\frac{\lambda_g(f_0)}{4}$	$1.2\,w_{t_{ms}}$	$\frac{a+w_{ti}}{2}$	$\frac{2}{l_t}$	$\frac{\lambda_{ms}(f_0)}{4}$	$4\,w_{tf}$

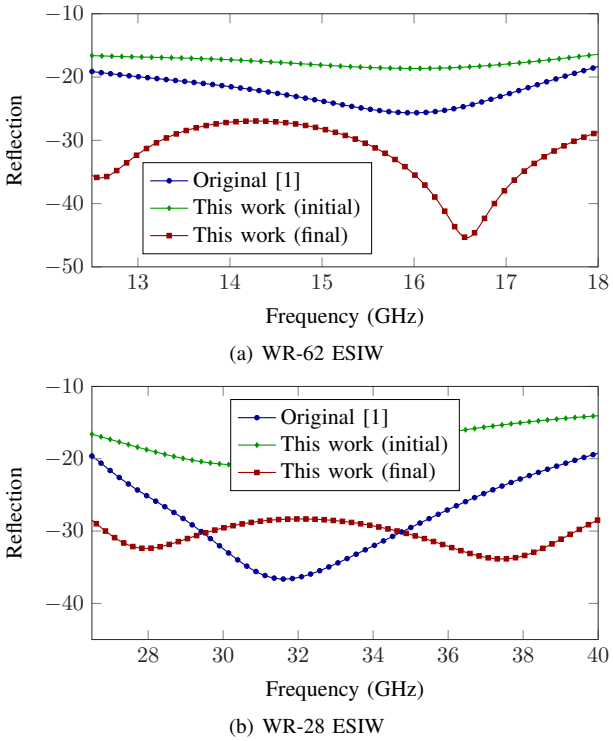
Table I. Initial values for the design parameters of the improved new microstrip to ESIW transition.

The expressions of table I have been used to design two transitions in a Rogers 4003 substrate of height $h = 0.508$ mm, permittivity $\varepsilon_r = 3.55$, and metal thickness $t = 35\,\mu$m. The first transition is for an ESIW with the same width as the standard WR-62 rectangular waveguide. The second transition is for an ESIW with the width of a WR-28 rectangular waveguide. Table II shows the values chosen for the fixed geometrical parameters, together with the initial values of the design parameters, obtained with the expression of table I,

	Fixed values (dimensions in mm)			
	WR-62		WR-28	
a	15.7988		7.1120	
h	0.5080		0.5080	
w_{ms}	1.1071		1.0673	
w_{tf}	0.5000		0.2500	
d_f	1.0000		1.0000	
d_v	0.7000		0.7000	
s_v	1.0000		1.0000	
	Optimization parameters (dimensions in mm)			
	WR-62		WR-28	
	Initial	Final	Initial	Final
l_t	6.4580	6.1568	2.9550	2.7440
w_{ti}	2.4000	2.3693	1.2000	1.5727
w_{ir}	9.0994	7.3651	4.1560	3.6127
$1/c$	3.2290	4.4745	1.4775	1.1324
$l_{t_{ms}}$	3.0000	3.9904	1.2980	1.3203
$w_{t_{ms}}$	2.0000	1.8088	1.0000	1.0331

Table II. Dimensions of the two designed transitions ($\epsilon_r = 3.55$).

and the final optimum values, obtained after fine-tuning with the Computer Simulation Technology (CST) commercial software, following an optimization process with the trust region algorithm. Thanks to the use of the good initial point, the optimization process is significantly reduced to less than 100 simulations.



(a) WR-62 ESIW

(b) WR-28 ESIW

Fig. 2. Reflection of the microstrip to ESIW transition. Comparison between original and new transitions (initial and optimum designs).

Figure 2 shows the reflection of the original transition of [1] and the transition presented in this work (both the initial and the optimum design). These results correspond to simulations made with CST. No losses have been considered. It can be observed that the initial point provides a good approximation

to the optimum values, with return losses above 15 dB. After the optimization, both transitions (for WR-28 and for WR-62) provide return losses over 28 dB in all the usable frequency band of the ESIW. It can also be observed that the improved new transition increases in 10 dB the minimum return losses when compared to the original transition.

III. Back-to-back prototype

Fixed values (dimensions in mm)		Optimization parameters (dimensions in mm)	
a	15.7988	l_t	5.9917
h	0.8130	w_{ti}	2.9469
w_{ms}	1.8519	w_{ir}	6.8070
w_{tf}	0.5000	$1/c$	3.8945
d_f	1.0000	$l_{t_{ms}}$	2.1756
d_v	0.7000	$w_{t_{ms}}$	2.4486
s_v	1.0000		

Table III. Dimensions of the manufactured taper ($\epsilon_r = 3.55$).

In order to test the validity of the improved new transition, a back-to-back transition has been designed and manufactured. A Rogers 4003 substrate with height $h = 0.813$ mm and $\varepsilon_r = 3,55$ has been chosen, so the transition is tested with a different substrate thickness than in the previous section, but it is still a value with which the original transition failed to provide good results. The ESIW used in this transition has the same width as the WR-62 waveguide. The design procedure described in the previous section has been used in order to design the microstrip to ESIW transition. The optimum geometrical values of the transition are shown in table III.

Fig. 3. Manufactured back-to-back transition without top and bottom covers.

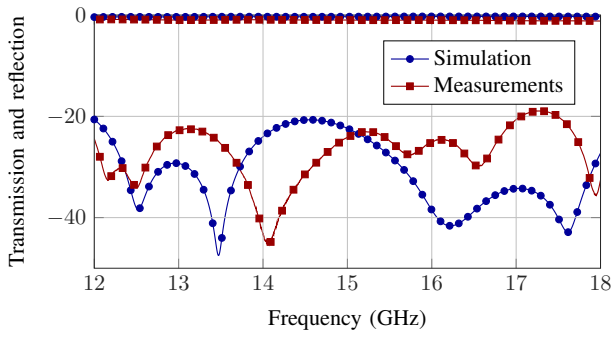


Fig. 4. Comparison between simulation and measurement for the back-to-back transition from microstrip to ESIW.

Figure 3 shows the manufactured prototype of the back-to-back transition without the top and bottom covers. After measuring with a TRL calibration kit, the measured transmission and reflection coefficients are depicted in figure 4, and compared with simulation. The simulated results have been obtained with CST, considering losses both in the metallic parts and in the dielectric body. As it can be observed, simulation and measurements are in good agreement. The measured return loss is greater than 20 dB and the insertion loss is smaller than 1.2 dB for the back to back (0.6 dB for only one transition) in the whole usable frequency band of the ESIW, while in [6] the return losses were 13.5 dB and insertion losses were 0.75 dB for one transition.

IV. Conclusions

In this work, a new microstrip to ESIW transition has been improved with via holes than prevent power leakage and two holes that ensure accuracy in the manufacturing of the input iris. A design procedure has been provided for this transition. The new design procedure has been successfully been used for designing two transitions in different frequency bands with thin substrates, and also for the design and manufacturing of a back to back transition in a thick substrate. Measured results of the back to back transition show a significant improvement in the return and insertion losses when compared to previously reported alternative solutions.

V. Acknowledgement

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