

High-performance Coplanar Waveguide to Empty Substrate Integrated Coaxial Line Transition

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Abstract—Recently, a new empty coaxial structure, entirely built with printed circuit boards, has been proposed. The resulting coaxial line has low radiation, low losses, high quality factor, and is non-dispersive. Up to now, this coaxial line has not been completely integrated in a planar substrate, since a working transition to a traditional planar line has not been defined yet. Therefore, in this paper, a high-quality transition from coplanar waveguide to this new empty coaxial line is proposed. With this transition, the coaxial line is completely integrated in a planar circuit board, so that it truly becomes an empty substrate-integrated coaxial line. The proposed transition has been fabricated. Both full-wave simulated and measured results show an excellent agreement. Therefore, the proposed transition is suitable to develop completely substrate-integrated components for applications in wideband communication systems that require very high-quality responses and protection from external interferences. To show this fact, this new transition has been applied to integrate a high-performance empty coaxial filter in a planar substrate. The measured response of this filter is excellent, and proves the goodness of the proposed transition that has enabled, for the first time, the complete integration of an empty coaxial line in a planar substrate.

Index Terms—Empty substrate integrated coaxial line, ESICL, substrate integrated coaxial line, SICL, substrate integrated waveguide, SIW, substrate integrated circuit, SIC, bandpass filter.

I. INTRODUCTION

INTTEGRATION of microwave/RF components in communication systems is of key importance to design and fabricate circuits with small size, low weight, low cost, high reliability, easy assembling and possibility of mass production. Full system integration is therefore playing an important role in current telecommunication developments. As a consequence, a great deal of effort has been dedicated to propose novel devices in planar technology. Some years ago, Deslandes and Wu [1] presented in 2001 an initial research work that gave and is giving rise to a vast number of new substrate integrated components. In this study, a novel concept for substrate integrated waveguide (SIW) transmission line was presented. The proposed structure employed rods of metallic via holes to confine a propagating wave between the upper and

bottom plates of a substrate layer. By this mean, the vertical dimension of a conventional 3D waveguide transmission line can be reduced. Thereafter and based on this former study, several solutions including filters [1]–[10], antennas [11]–[16], transitions and tapers [17]–[19], baluns [20], [21], couplers [22]–[25] and new transmission lines [26]–[30] were proposed. Among all these works, it is of interest the excellent properties of substrate integrated coaxial lines (SICL) reported in [30]. This transmission line was shown to have single mode propagation, non-dispersion and low radiation. Due to these properties, this sort of coaxial line can be suitable for applications with wider bandwidth responses and lower losses than other proposed substrate integrated circuits. For instance, wideband filters [31], [32], couplers [33], [34], baluns [35] and power dividers [36] have been designed using SICLs.

In all the aforementioned structures, the substrate integrated design offers a range of benefits in comparison with conventional 3D waveguide and coaxial transmission lines. However, the losses introduced by the dielectric permittivity of the substrate limit the use of these devices, specially as frequency is increased. This fact was clearly demonstrated in the work presented by Belenguer et al. [37]. In this particular case, the proposed structure, called empty substrate integrated waveguide (ESIW), showed significantly lower insertion loss than SIW for two bandpass filter designs working at different frequencies. In addition, it was also shown that the quality factor is increased around 8 times due to the absence of dielectric material.

Following the same idea, in [38] an empty coaxial line is proposed. This coaxial line is entirely built using printed circuit boards (PCBs), but, strictly speaking, it is not integrated in a dielectric substrate since, in this work, it has not been proposed a transition to, at least, one traditional planar transmission line: microstrip, coplanar waveguide, stripline, etc. [39]. However, the complete integration of this empty coaxial line is of great interest for developing high-quality, low-cost and shielded integrated microwave devices. Therefore, we present in this paper a transition from grounded coplanar waveguide (GCPW) to this new empty coaxial transmission line. The integration of a coaxial line into a partially empty substrate permits to obtain non-dispersive and shielded lines with low loss, low radiation and suitable for wideband applications. Microstrip or coplanar lines are low cost and straightforward to fabricate, but are not shielded and exhibit radiation losses and cross-talk problems. On the other hand, striplines present lateral leakage in addition to cross-talk. The proposed coaxial topology solves these drawbacks and combines the advantages

This work was supported by the Ministerio de Economía y Competitividad, Spanish Government, under Research Projects TEC2013-47037-C5-3-R and TEC2013-47037-C5-1-R.

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of coaxial cables and planar transmission lines. Also, it permits to easily control the dimensions of the coaxial line. As a result, the impedance of the line can be adjusted modifying the widths of the inner and outer conductors, or even loading these conductors with inductive/capacitive elements as well as tunable components to obtain reconfigurable responses. The proposed design has the advantage of fast full-wave simulation as a PEC (perfect electric conductor) background material can be used during calculations. This is not possible for open structures, where a radiation boundary condition is necessary. This fact considerably reduces the computation time, which is of great importance during optimization processes (e.g. for design purposes).

To show one possible application of the proposed transition to this new empty substrate integrated coaxial line (ESICL), a wideband bandpass filter is designed and fabricated. In this regard, it is important to note that this bandpass filter response cannot be obtained with SIW/ESIW structures, and has several advantages compared to microstrip, coplanar or stripline filters such as non-radiation, non-dispersion, non-crosstalk, faster simulation and lower insertion loss. The proposed coaxial line has a wide range of potential applications. For instance, communication systems incorporating services that operate in a wide band and that requires protection from external electromagnetic interferences.

The paper is organized as follows. Section II presents the layout, design and performance of the coaxial line. Section III presents a high-performance GCPW to ESICL transition. The response of a bandpass filter prototype is shown in Section IV. The experimental results are presented in section V. Finally, the main conclusions of the work are discussed in Section VI.

II. ESICL ASSEMBLING AND PERFORMANCE

At least three substrate layers plus two covers, which close the whole structure, are required to fabricate an ESICL (see Fig. 1). One or more inner layers, which must be separated from the covers by, at least, one substrate layer, sustain the internal conductor of the coaxial line as it is shown in Fig. 1. The covers can be manufactured by simply using thin metallic sheets, or they can be built using two additional substrate sheets, which would allow to integrate external circuitry or lumped elements that could interact with the ESICL device.

The different layers of this structure can be of different thickness and material, but, in any case, they can be entirely fabricated using standard PCB fabrication processes. Once the different layers have been manufactured, the structure can be easily assembled. In order to prevent misalignment errors, a set of screws has been distributed uniformly along the structure with excellent results (see section V). These screws can be maintained and used to join the different layers by pressure. Due to the current distribution of the coaxial line, this gives very good results. The different ESICL layers can be also assembled using soldering paste, which is a standard process in PCB fabrication and could be easily automated, providing better metallic contact and lighter devices, since, in this case, the alignment screws can be removed. Both assembling strategies provide excellent results.

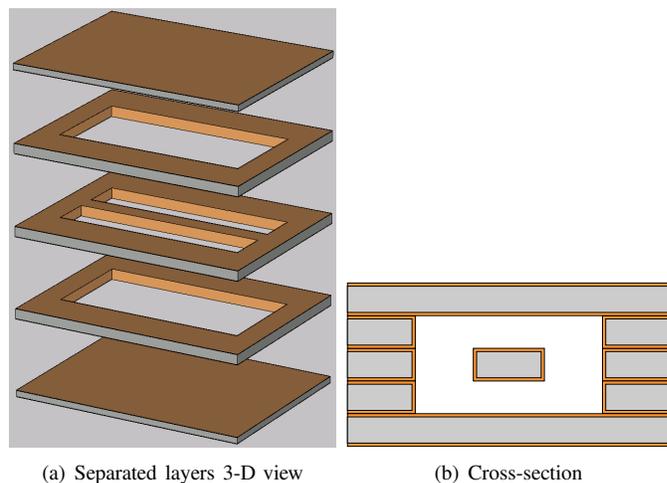


Fig. 1. Simplest construction of an ESICL (three inner substrate layers plus two covers).

TABLE I
SIMULATED LOSSES AND UNLOADED Q FACTORS OF SEVERAL WELL-KNOWN TRANSMISSION LINES AND ESICL. SUBSTRATE (IF APPLIES): ROGERS 4003C ($h = 0.813$ MM, $\epsilon_r = 3.55$, AND $\tan \delta = 0.0027$). METALIZATION: PLAIN SOLID COPPER ($\sigma = 5.8 \cdot 10^7$ S/M)

Line	Dimensions	Losses (15 GHz)	Q_u (15 GHz)
RWG	$a = 15.7988$ mm $b = 7.8994$ mm	0.17 dB/m	6134.1
ESIW	$a = 15.7988$ mm $b = 0.933$ mm	1.07 dB/m	1487.1
SIW	$a = 8.3851$ mm $b = 0.933$ mm	11.06 dB/m	288.03
Microstrip	$w_{strip} = 1.97$ mm	7.79 dB/m	23.07
GCPW	see feeding line in Fig. 3	9.23 dB/m	152.34
ESICL	$w_{inner} = 1.917$ mm $h_{inner} = 0.933$ mm $w_{outer} = 6$ mm $h_{outer} = 2.799$ mm	0.9 dB/m	1567.7

In order to evaluate the performance of the ESICL, in Tab. I, the losses of an ESICL are compared, at 15 GHz, with the losses of several transmission lines: microstrip, GCPW, SIW, ESIW, and rectangular waveguide (RWG). These losses have been computed from full-wave simulations using the commercial software CST Studio Suite 2014. The dimensions for all of the compared lines are also shown in Tab. I. These dimensions have been determined considering the following facts: the planar lines have been devised for a Rogers 4003C substrate of 0.813 mm thickness and 35 μm of metallization, the QTEM/TEM lines have been designed to exhibit a characteristic impedance of 50 Ω , and, finally, the waveguides have been designed to match the desired bandwidth, from 12 to 18 GHz.

Additionally, in order to provide a more exhaustive comparison of the performance of these lines, the unloaded Q factor of a $\lambda/2$ resonator has been also estimated. To perform this analysis, a piece of the lines of Tab. I, of length approximately equal to $\lambda/2$, has been tightly coupled to identical feeding

lines, so that the desired resonator has been obtained. A capacitive gap has been used to couple the feeding lines and the resonator for the QTEM/TEM lines, i.e. microstrip, GCPW, and ESICL, while an inductive iris has been used to couple the feeding lines to the resonator for the waveguides, i.e. RWG, ESIW, and SIW. These resonators have been simulated with CST Studio Suite 2014, and then the unloaded Q factor has been estimated applying the following formula [40],

$$Q_u = \frac{f}{\frac{f_H - f_L}{1 - 10^{-IL/20}}} \quad (1)$$

where f is the resonant frequency, $f_H - f_L$ is the half-power bandwidth, and IL is the insertion loss at f .

The performance of the ESICL is comparable to ESIW, quite close to the performance of the rectangular waveguide, and much higher than the performance of classical planar lines like microstrip or GCPW, or even SIW, which is considered a high-performance planar line. Therefore, very high quality devices can be designed using this novel and promising transmission line.

III. GCPW-TO-ESICL TRANSITION

Without a proper transition to a traditional planar line, the usefulness of the ESICL is very limited. Therefore, in this section, a high-quality transition to a GCPW line has been designed [41]. In Fig. 2, a 3D-view of this new transition without covers is shown. In this figure it can be seen that,

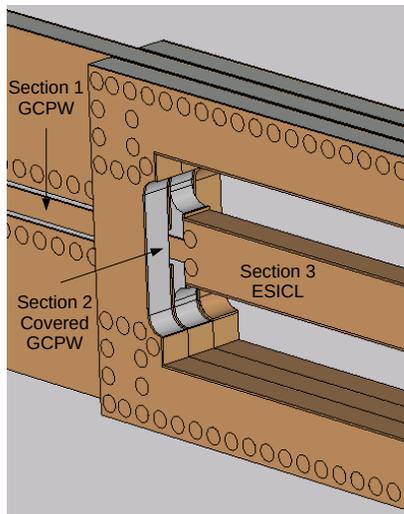


Fig. 2. 3-D detail of a complete GCPW-to-ESICL transition without covers.

globally, the transition consists of three different sections. The first section is simply the GCPW feeding line. The second section is also a GCPW line, but, in this case, covered with a dielectric and surrounded by a metallic housing. Finally, the third section is the ESICL itself.

In Fig. 3, it can be seen the top and bottom view of the transition for the central substrate layer, which sustains the inner conductor of the coaxial line. In this figure, only the separation between the vias surrounding the coplanar waveguide has been specified, p_{cop} . The other vias simply

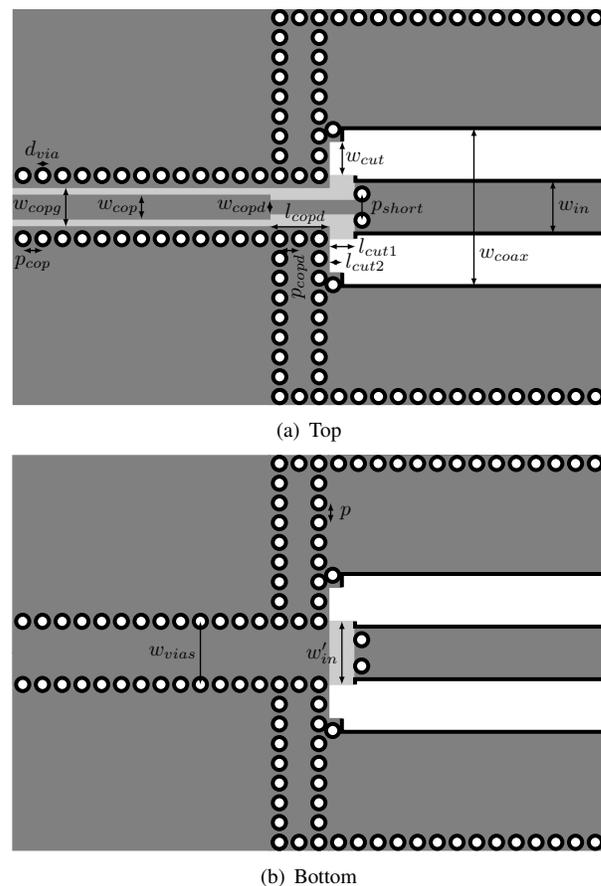


Fig. 3. GCPW-to-ESICL transition in the central layer. Dark gray is metal covering the substrate. White represents holes emptied in the substrate. Light gray stands for substrate without metallic cover. Black represents the metallization along substrate edges.

shield the structure and they barely affect the response of the transition. Therefore, it is not necessary to give a fixed value for their separation, p . Its actual value depends on the width of the substrate layer for the vertical rows of vias, and the length of the ESICL for the horizontal rows. Nevertheless, p is always chosen as close as possible to p_{cop} .

In Fig. 4, it is shown the layout of the substrate sheet that is placed above the main substrate layer of Fig. 3.

In this layer, the transition is quite simpler. A frame around the hole that defines the coaxial line is necessary in order to provide mechanical stability to the whole structure. Due to this necessary frame, the line that crosses below it, in the central layer, becomes a CGPW covered with dielectric and metal, leading to the second section of the transition. In order to keep the same line impedance in this second section of the transition, the central strip of the covered GCPW is slightly narrower than the central strip of the conventional GCPW feeding line.

In Fig. 5, one can see the transition in the lower layer, which is the simplest one. In this case, a frame of dielectric material is also necessary to provide the structure with the necessary mechanical stability. However, in this case, the presence of this external frame has no consequence from the electromagnetic point of view.

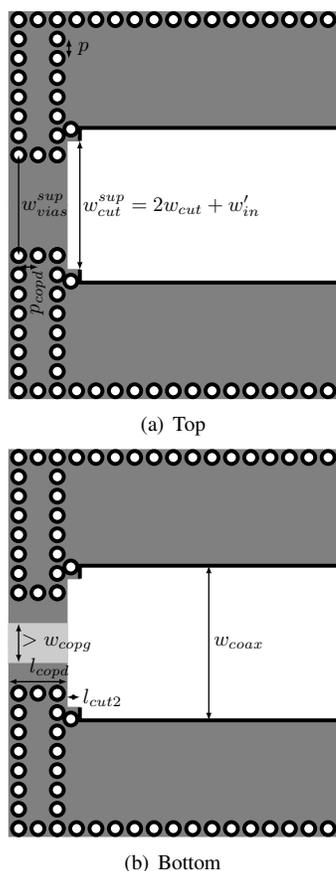


Fig. 4. GCPW-to-ESICL transition in the upper layer. Dark gray is metal covering the substrate. White represents holes emptied in the substrate. Light gray stands for substrate without metallic cover. Black represents the metallization along substrate edges.

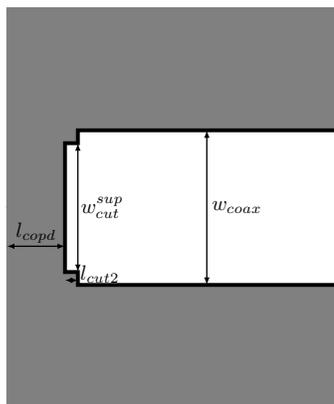


Fig. 5. GCPW-to-ESICL transition in the lower layer. Dark gray is metal covering the substrate. White represents holes emptied in the substrate. Black represents the metallization along substrate edges.

Finally, an specific transition has been designed. This transition has been optimized for a Rogers 4003CTM substrate ($\epsilon_r = 3.55$, 0.813 mm thickness and 35 μm of copper metallization). In this case, all of the layers that form this structure have been implemented using the same substrate, although a cheaper substrate, for example FR-4, could have been used to build the lower layer and the covers. The dimensions of the designed

TABLE II
DIMENSIONS FOR THE TRANSITION IN ROGERS 4003CTM ($\epsilon_r = 3.55$,
 $h = 0.813$ mm)

$d_{via} = 0.5$ mm	$p_{cop} = 0.714$ mm
$w_{copg} = 1.014$ mm	$w_{vias} = 1.914$ mm
$w_{cop} = 0.714$ mm	$w_{copd} = 0.637$ mm
$l_{copd} = 2$ mm	$p_{copd} = 0.667$ mm
$w'_{in} = 2.117$ mm	$w_{cut} = 1.162$ mm
$l_{cut1} = 0.526$ mm	$l_{cut2} = 0.5$ mm
$p_{short} = 0.806$ mm	$w_{in} = 1.917$ mm
$w_{coax} = 6$ mm	$w_{vias}^{sup} = 4.44$ mm

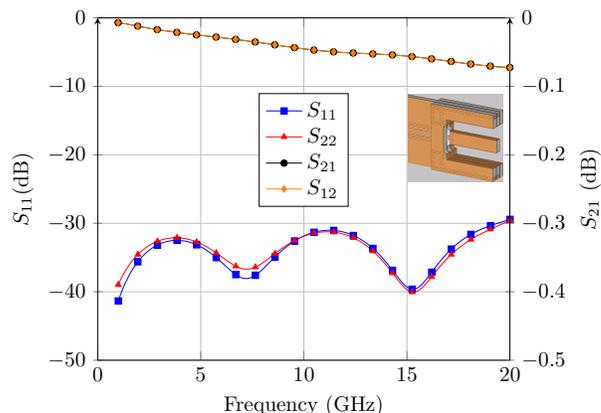


Fig. 6. Simulated response with a full-wave 3-D electromagnetic simulator of the designed GCPW-to-ESICL transition.

transition can be read in Tab. II.

The procedure followed to design this transition is quite simple. In the first place, the lines are designed separately: the feeding GCPW, the covered GCPW, and the ESICL, so that all of them have the same characteristic impedance (50 Ω in this case). The dimensions obtained in this first step are translated to the structure. Then, the transition is optimized with a full 3-D electromagnetic simulator for: w_{cut} , w_{copd} and l_{cut1} , so that the return losses are maximized in the band of interest (in this case from 0 to 20 GHz).

In Fig. 6, one can see the simulated response for the transition using a full-wave 3D electromagnetic software and considering losses. This transition exhibits an excellent response in the band of interest (0-20 GHz) and a really low loss level (0.07 dB at 20 GHz). The ESICL and this new transition are quite easy to fabricate, since only standard printed circuit board (PCB) manufacturing processes are involved in its fabrication, i.e. milling, cutting, drilling and plating. Thanks to this transition, it has been possible to completely integrate an actual TEM line (not QTEM) in a planar substrate. Most of the traditional design methods conceived for planar TEM or QTEM lines (microstrip, coplanar, stripline ...) are based on the assumption that the line supports the propagation of a pure TEM mode. Therefore, they can be applied to this new transmission line, and, indeed, since this line is actually a TEM line, the results obtained will be even more accurate than the results obtained for QTEM lines. On the other hand, it is necessary to remark that ESICL is a line that exhibits very low losses. Devices implemented in ESICL, mainly those incorporating resonators, will provide very high-quality

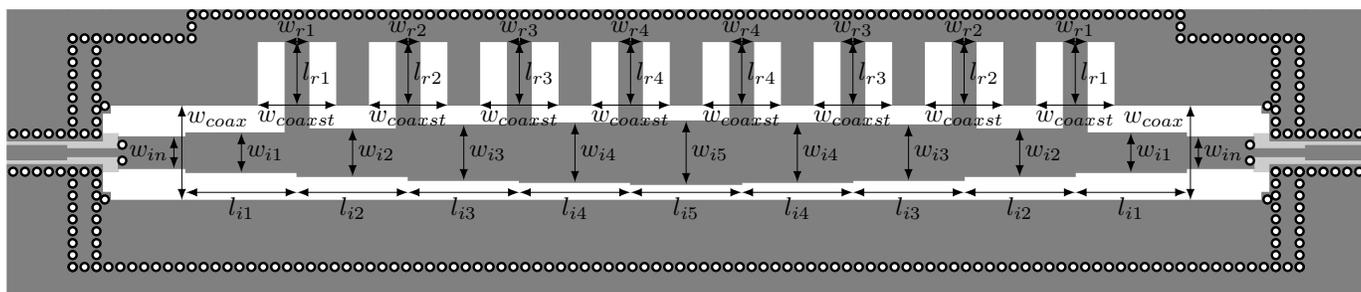


Fig. 7. Top view and dimensions for the eight cavity filter in ESICL.

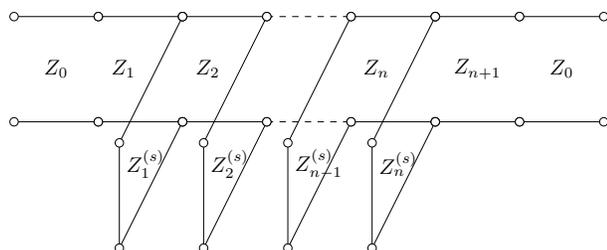


Fig. 8. Bandpass filter with shorted stubs.

TABLE III
DIMENSIONS FOR THE EIGHT CAVITY FILTER IN ESICL.

$w_{in} = 1.917$ mm	$w_{coax} = 6$ mm	$w_{coaxst} = 5$ mm
$w_{i1} = 2.583$ mm	$w_{i2} = 3.833$ mm	$w_{i3} = 3.771$ mm
$w_{i4} = 3.649$ mm	$w_{i5} = 3.519$ mm	$l_{i1} = 7.446$ mm
$l_{i2} = 8.330$ mm	$l_{i3} = 8.109$ mm	$l_{i4} = 7.999$ mm
$l_{i5} = 7.941$ mm	$l_{r1} = 6.319$ mm	$l_{r2} = 6.432$ mm
$l_{r3} = 6.403$ mm	$l_{r4} = 6.396$ mm	$w_{r1} = 1.671$ mm
$w_{r2} = 1.683$ mm	$w_{r3} = 1.895$ mm	$w_{r4} = 1.709$ mm

responses since the ESICL resonators will have very high quality factors. The response of these new ESICL devices will be undoubtedly much better than the responses that could be obtained with any conventional planar line.

IV. BANDPASS FILTER

In order to show the integration capabilities of the proposed transition, a real device will be fully integrated in a printed circuit board. In parallel, the performance of this real device will be also evaluated, in order to remark the interest of the proposed transition, since it will allow to integrate high-quality and completely shielded devices in a traditional PCB.

Specifically, a very wide-band filter will be integrated in a Rogers 4003C substrate ($\epsilon_r = 3.55$, 0.813 mm thickness and 35 μm of copper metallization). This filter exhibits a fractional bandwidth of 100%, a central frequency, $f_0 = 10$ GHz, and a passband ripple of 0.05 dB. In order to design this filter, a traditional configuration for designing wide-band bandpass filters with planar lines has been applied [42]. In this configuration, the resonators of the filter have been implemented with shorted stubs of length equal to $\lambda/4$. These resonators have been coupled through impedance inverters, which have been synthesized with line sections of length equal to $\lambda/4$ (see figures 7 and 8).

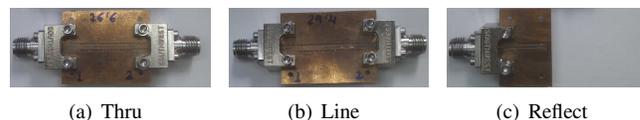


Fig. 9. Custom calibration kit used to de-embed the coaxial connectors from measurements.

The dimensions of the filter can be seen in Fig. 7 and Tab. III. In this figure, one can see that the filter is indeed the direct implementation in ESICL of the filter of Fig. 8. This filter can be analyzed as a closed and empty structure. The size of the problem is electromagnetically small, so that it can be analyzed very fast. In this case, optimization is possible even with a commercial full-wave electromagnetic software. Therefore, it has been possible to tune the response of the filter, which ends up being very close to the response of the filter prototype, as it can be seen in the simulated results of Fig. 12. These results are undoubtedly excellent, since they consider the losses produced by the whole device. These losses are very small, only 0.14 dB at f_0 .

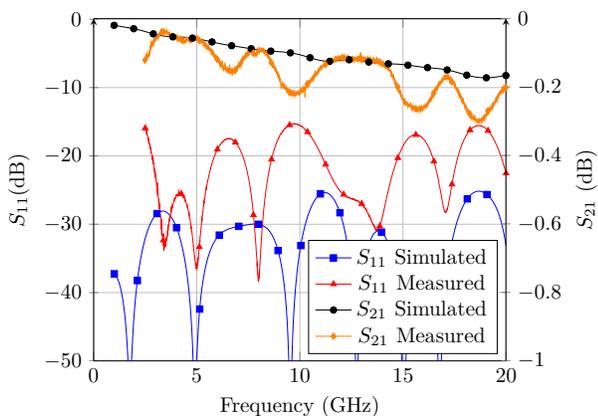
V. RESULTS

In order to experimentally verify the simulated results of the previous sections, the back-to-back configuration for the transition (Fig. 10) and the filter (Fig. 11) have been fabricated.

To connect the fabricated prototypes with the vector network analyzer, K coaxial connectors have been used. Since these connectors can degrade the measured results, they have been de-embedded from measurements using a TRL calibration kit. This kit is composed of a GCPW transmission line of 29.4 mm (Line), a shorter transmission line of 26.6 mm (Thru) and a shorted line of 13.3 mm (Reflect). The photographs of these calibration standards are shown in Fig. 9.

In Fig. 10, it can be seen a comparison between measurements and the simulated results for the back-to-back of the proposed transition. Although, due to fabrication tolerances, the measured response has deteriorated, the line is still very well integrated in the PCB and, therefore, it can be concluded that the main objective of this work has been accomplished, i.e. the complete integration of the novel ESICL line in a dielectric substrate.

In order to determine the extent to which the fabrication tolerances affect the quality of the transition, a yield analysis has been performed using CST Studio Suite 2014. In this



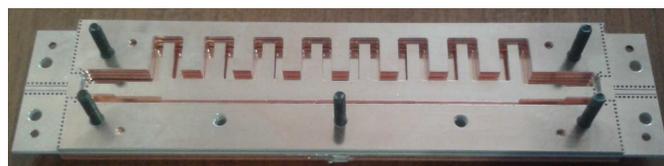
(a)



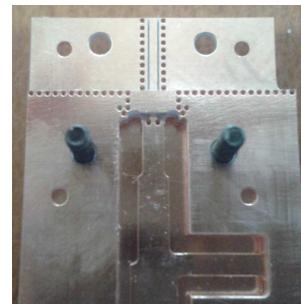
(b)

Fig. 10. (a) Simulated response with a full-wave 3-D electromagnetic simulator vs. measurements (de-embedded to the GCPW) for the back-to-back of the GCPW-to-ESICL transition. (b) Photograph of the bak-to-back.

analysis, it has been considered that the positions of several key faces of the whole structure admit certain degree of error. In this context, the most sensitive design parameters of the transition are those that affect the impedance of the lines. For example, it has been considered that the lateral limits of the central strip, which determine the impedance of the second section of the transition (a covered GCPW), can vary its position following a normal distribution with zero mean (the design position) and a standard deviation of 25 microns (the typical error we have observed for milled geometries). Other sensible faces in this design have been included in the yield analysis: the outer walls that laterally close the ESICL with a standard deviation of 50 microns (cutters are less precise than mills), the lateral walls of the internal conductor of the ESICL with a standard deviation of 50 microns, the upper and lower walls of the inner conductor of the ESICL with a standard deviation of 50 microns, and finally the position of the upper and lower walls that close the ESICL (the total height of the line) with a standard deviation of 100 microns, since the actual height of the line is affected by many factors: the actual height of the substrates, the actual metallization depth, and imperfections that prevent the different layers to match perfectly. The results of the yield analysis show that: 99.9% of the back-to-back realizations will exhibit return losses greater than 10 dB, 96.7% will exhibit return losses greater than 15 dB, and 79.1% will exhibit return losses greater than 20 dB. Of course, this is a very complex design and it is impossible to perform a full yield analysis considering all the possible errors, but, since the selected dimensions are the most critical ones, the results given by this analysis could be considered a very good approximation of the fabrication process performance.



(a)



(b)

Fig. 11. (a) Photograph of the manufactured ESICL filter. (b) Detail of the transition which has been used to feed the filter prototype.

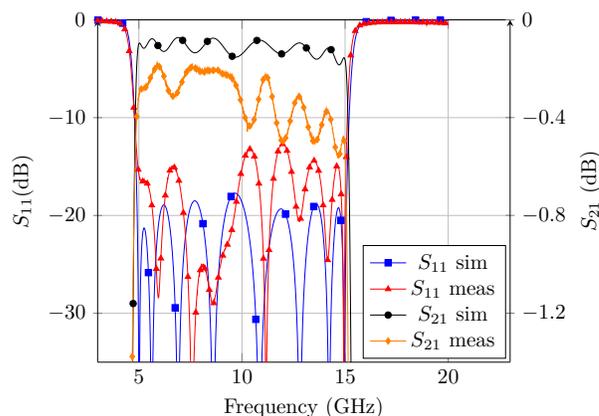


Fig. 12. Simulated response with CST (FEM solver) and measurements (de-embedded to the GCPW) for the eight cavity ESICL filter.

In Fig. 11(a), it is shown a photograph of the filter prototype without the upper cover. Besides, in Fig. 11(b), it can be seen a detailed view of one of the transitions that feed the aforementioned prototype. Finally, in Fig. 12, one can see a comparison between simulations and measurements. In this figure, both results, experimental and simulated, exhibit a high degree of coincidence, although, again, the adaptation is slightly deteriorated in measurements. Results, simulations without considering the GCPW-to-ESICL transitions, and measurements including both transitions, prove that the new transition barely affects the response of the filter, i.e. both show very similar levels of insertion loss. This fact validates again the transition, and confirms that the main objective of this work has been accomplished, since these new ESICL devices can be easily integrated in a traditional PCB.

VI. CONCLUSIONS

The ESICL is a novel structure that can be entirely fabricated with standard dielectric substrate layers, and exclusively

using PCB standard manufacturing procedures. This structure shows very interesting properties, i.e. low-loss, non-dispersion, immunity to interferences or cross-talk, etc., which makes it very attractive for developing high-quality passive or active devices. In this paper, for the first time, a high-performance transition from a traditional planar transmission line, a GCPW, to the novel ESICL has been designed. As a result, the promising ESICL has been, for the first time, successfully and truly integrated in a planar substrate. In order to illustrate this fact, a wide band (100% fractional bandwidth) bandpass eight cavity filter in ESICL has been designed and, using this new transition, integrated in a planar substrate. The filter exhibits a very high-quality response in the whole band of interest, with measured insertion losses of 0.23 dB at 11.15 GHz (considering both feeding GCPW-to-ESICL transitions). The results presented in this paper are very promising, and open a wide range of possibilities to develop high-quality PCB-integrated devices in ESICL exhibiting: very low losses, wide working bandwidths, high stability, and immunity to interferences, cross-talk and dispersion.

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